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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,620	11/13/2003	Ryuji Nishikawa	YKI-0139	2386

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EXAMINER	
SANEI, HANA ASMAT	
ART UNIT	**PAPER NUMBER**
2879	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/713,620	NISHIKAWA, RYUJI	
	Examiner	Art Unit	
	Hana A. Sanei	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13 November 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The Declaration, filed on March 24, 2004, has been entered and acknowledged by the Examiner.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

4. Applicant is reminded of the proper format for an abstract of the disclosure.

The abstract should be generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 & 4-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (EP 1032045 A2).

With respect to Claim 1, Yamada discloses an organic electroluminescence panel (Figure 6B) in which a plurality of organic electroluminescence elements are formed above a substrate, each organic electroluminescence element including at least an organic layer including an organic emissive material (163) between a lower individual electrode (anode, 161) which is individually patterned for each pixel and an upper electrode (cathode, 166), the organic electroluminescence panel comprising: an edge covering insulating layer (innermost portion of the planarization insulation layer, 167) for covering peripheral end portions of the lower individual electrode, and a mask supporting insulating layer (outermost portion of the planarization insulation layer, 167; Col.11, lines 56-58 – Col. 12, lines 1-9), which is formed on an outer peripheral region with respect to the edge covering insulating layer and has a greater thickness than the edge covering insulating layer (167), for supporting a mask, which is used when forming the organic layer, on a top surface thereof, wherein the organic layer (163) terminates on an outer region with respect to the boundary between the edge covering insulating layer and the lower individual electrode (Figure 6B), and on an inner region with respect to a region where the mask supporting insulating layer is formed, and the organic layer is individually patterned for each pixel (Figure 6B).

With respect to Claim 4, Yamada discloses that the edge covering insulating layer and the mask supporting insulating layer are formed by

patterning a single insulating layer (165). Furthermore, Examiner notes that the method of forming the edge covering insulating layer and the mask supporting insulating layer, i.e. "by patterning a single insulating layer in respective predetermined patterns having different thicknesses by means of multi-phase exposure or gray-tone exposure", is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given any patentable weight.

With respect to Claim 5, Yamada discloses an organic electroluminescence panel (Figure 6B) in which a plurality of organic electroluminescence elements are formed above a substrate, each organic electroluminescence element including at least an organic layer including an organic emissive material (163) between a lower individual electrode (anode, 161) which is individually patterned for each pixel and an upper electrode (cathode, 166), the organic electroluminescence panel comprising: an edge covering insulating layer (innermost portion of the planarization insulation layer, 167) for covering peripheral end portions of the lower individual electrode, and a upper insulating layer (outermost portion of the planarization insulation layer, 167; Col.11, lines 56-58 – Col. 12, lines 1-9), which is formed on an outer peripheral region with respect to the edge covering insulating layer and has a greater thickness than the edge covering insulating layer (167), wherein the organic layer (163) terminates on an outer region with respect to the boundary between the edge covering insulating layer and the lower individual electrode (Figure 6B), and on an inner region with respect to a region where the upper

insulating layer is formed, and the organic layer is individually patterned for each pixel (Figure 6B).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada (US 6768257 B1).

With respect to Claim 1, Yamada discloses an organic electroluminescence panel (Figure 6) in which a plurality of organic electroluminescence elements are formed above a substrate, each organic electroluminescence element including at least an organic layer including an organic emissive material (11) between a lower individual electrode (anode, 10) which is individually patterned for each pixel and an upper electrode (cathode, 12), the organic electroluminescence panel comprising: an edge covering insulating layer (insulating film, 13) for covering peripheral end portions of the lower individual electrode, and a mask supporting insulating layer (rib, Figure 5C, #14; Col. 6, lines 40-46) which is formed on an outer peripheral region with respect to the edge covering insulating layer and has a greater thickness than the edge covering insulating layer, for supporting a mask, which is used when forming the organic layer, on a top surface thereof, wherein the organic layer (11) terminates on an outer region with respect to the boundary between the edge covering insulating layer and the lower individual electrode (Figure 6), and on an

inner region with respect to a region where the mask supporting insulating layer is formed and the organic layer is individually patterned for each pixel (Figure 6).

With respect to Claim 2, the Examiner notes that the method of forming a hole injection layer (Figure 6, #11, Col. 7, lines 20-29) and an organic emissive layer, i.e. "by vacuum evaporation", is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given any patentable weight. Yamada discloses that each of the hole injection layer (Figure 6, #11, Col. 7, lines 20-29) and the organic emissive layer terminates on the inner region with respect to a region where the mask supporting insulating layer is formed. (Figure 6, #11)

With respect to Claim 3, Yamada discloses a charge transport layer (electron transport layer, Col. 7, lines 17-29) is formed between the organic emissive layer (light emitting layer, Col. 7, lines 23-24) and the upper electrode (12), and the charge transport layer terminates on the outer region with respect to the boundary between the edge covering insulating layer and the lower individual electrode, and on the inner region with respect to a region where the mask supporting insulating layer is formed, and the charge transport layer is individually patterned for each pixel (Figure 6).

With respect to Claim 4, the Examiner notes that the method of forming the edge covering insulating layer and the mask supporting insulating layer, i.e. "by patterning a single insulating layer in respective predetermined patterns having different thicknesses by means of multi-phase exposure or gray-tone

exposure", is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given any patentable weight.

With respect to Claim 5, Yamada discloses an organic electroluminescence panel (Figure 6) in which a plurality of organic electroluminescence elements are formed above a substrate, each organic electroluminescence element including at least an organic layer including an organic emissive material (11) between a lower individual electrode (anode, 10) which is individually patterned for each pixel and an upper electrode (cathode, 12), the organic electroluminescence panel comprising: an edge covering insulating layer (insulating film, 13) for covering peripheral end portions of the lower individual electrode, and a upper insulating layer (rib, Figure 5C, #14; Col. 6, lines 40-46) which is formed on an outer peripheral region with respect to the edge covering insulating layer and has a greater thickness than the edge covering insulating layer, wherein the organic layer (11) terminates on an outer region with respect to the boundary between the edge covering insulating layer and the lower individual electrode (Figure 6), and on an inner region with respect to a region where the upper insulating layer is formed and the organic layer is individually patterned for each pixel (Figure 6).

With respect to Claim 6, the Examiner notes that the method of forming a hole injection layer (Figure 6, #11, Col. 7, lines 20-29) and an organic emissive layer, i.e. "by vacuum evaporation", is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given any patentable weight. Yamada discloses that each of the hole injection layer (Figure 6, #11,

Col. 7, lines 20-29) and the organic emissive layer terminates on the inner region with respect to a region where the mask supporting insulating layer is formed. (Figure 6, #11)

With respect to Claim 7, Yamada discloses a charge transport layer (electron transport layer, Col. 7, lines 17-29) is formed between the organic emissive layer (light emitting layer, Col. 7, lines 23-24) and the upper electrode (12), and the charge transport layer terminates on the outer region with respect to the boundary between the edge covering insulating layer and the lower individual electrode, and on the inner region with respect to a region where the mask supporting insulating layer is formed, and the charge transport layer is individually patterned for each pixel (Figure 6).

With respect to Claim 8, the Examiner notes that the method of forming the edge covering insulating layer and the mask supporting insulating layer, i.e. "by patterning a single insulating layer in respective predetermined patterns having different thicknesses by means of multi-phase exposure or gray-tone exposure", is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given any patentable weight.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9,11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 6768257 B1) in view of Yamagata et al. (US 6720198 B2).

With respect to Claim 9, Yamada discloses an organic electroluminescence panel (Figure 6) in which a plurality of organic electroluminescence elements are formed above a substrate, each organic electroluminescence element including at least a hole injection layer (Figure 6, #11, Col. 7, lines 20-29) and an organic emissive material (11) between a lower individual electrode (anode, 10) which is individually patterned for each pixel and an upper electrode (cathode, 12), the organic electroluminescence panel comprising: an edge covering insulating layer (insulating film, 13) for covering peripheral end portions of the lower individual electrode, and a mask supporting insulating layer (rib, Figure 5C, #14; Col. 6, lines 40-46) which has a greater thickness than the edge covering insulating layer, and has a greater thickness than the edge covering insulating layer, for supporting a mask, which is used when forming the organic layer, on a top surface thereof, wherein the organic emissive layer (11) is formed between the upper electrode and the hole injection layer and terminates on an outer region with respect to the boundary between the edge covering insulating layer and the lower individual electrode, and on an inner region with respect to a region where the mask supporting insulating layer is formed, and the organic emissive layer is individually patterned for each pixel (Figure 6; Col. 7, lines 17-29). Yamada is silent regarding that the hole injection layer is formed covering the lower individual electrode, the edge covering

insulating layer, and the mask supporting insulating layer. In the same field of endeavor, Yamagata teaches that the hole injection layer is formed covering the lower individual electrode, the edge covering insulating layer, and the mask supporting insulating layer (Figure 2, # 206; Col. 2, lines 5-18) in order to ensure proper generation of holes. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the structure of the hole injection layer, as disclosed by Yamagata, in the organic electroluminescence pane of Yamada. Motivation to combine would be to ensure proper generation of holes.

With respect to claim 11, Yamada discloses a charge transport layer (electron transport layer, Col. 7, lines 17-29) is formed between the organic emissive layer (light emitting layer, Col. 7, lines 23-24) and the upper electrode (12), and the charge transport layer terminates on the outer region with respect to the boundary between the edge covering insulating layer and the lower individual electrode, and on the inner region with respect to a region where the mask supporting insulating layer is formed, and the charge transport layer is individually patterned for each pixel (Figure 6).

With respect to Claim 12, the Examiner notes that the method of forming the edge covering insulating layer and the mask supporting insulating layer, i.e. "by patterning a single insulating layer in respective predetermined patterns having different thicknesses by means of multi-phase exposure or gray-tone exposure", is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given any patentable weight.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 6768257 B1) in view of Yamagata et al. (US 6720198 B2) with further consideration of Ogura et al. (US 2002/0070663 A1).

With respect to Claim 10, Yamada-Yamagata teaches the invention set forth above (see rejection in Claim 9 above) and further teaches that the hole injection layer and the organic emissive layer have specific thicknesses. Yamada-Yamagata is silent regarding that the hole injection layer has a thickness which is smaller than 10 nm, and the organic emissive layer has a total thickness of 10 nm or greater. In the same field of endeavor, Ogura teaches that the hole injection layer has a thickness which is smaller than 10 nm (Page 9, Par [0141] & Page 10, Par [0145]), and the organic emissive layer has a total thickness of 10 nm or greater (Page 9, Par [0140] in order to ensure good injection efficiency. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the thicknesses of the hole injection layer and the organic emissive layer, as disclosed by Ogura, in the organic electroluminescence panel of Yamada-Yamagata. Motivation to combine would be to ensure good injection efficiency.

Other Prior Art Cited

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Yamada (US 6366025 B1)

Yamazaki et al. (US 20030089991 A1)

Matsuoka et al. (US 20020192576 A1)

Yamada et al. (EP 1006587 A2)

Yamagata et al. (US 6720198 B2)

Yamazaki et al. (US 6852997 B2)

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hana A. Sanei whose telephone number is (571) 272-8654. The examiner can normally be reached on Monday- Friday, 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Hana A. Sanei

Karabi Guharay
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PRIMARY EXAMINER